CLAIMS

What is claimed is:

1. A cache memory comprising:

a general-purpose sector, the general-purpose sector to be used for general computer operations; and

a dedicated sector, the dedicated sector to be dedicated to a first computer process.

2. The cache memory of claim 1, wherein the dedicated sector is allocated to a first program thread.

3. The cache memory of claim 2, wherein the first program thread comprises a multi-media process.

4. The cache memory of claim 1, wherein the dedicated sector may be dynamically created or eliminated.

5. The cache memory of claim 4, wherein the size of the dedicated sector may be dynamically modified.

6. The cache memory of claim 1, wherein the first computer operation is allocated certain process times.

7. A processor comprising:

a processor core;

a first cache memory for general-purpose operation; and

a second cache memory dedicated to a first computer process.

8. The processor of claim 7, wherein first computer process is a multi-media process.

9. The processor of claim 7, wherein the first computer process is allocated certain computing cycles of the processor.

10. The processor of claim 7, wherein the first cache memory comprises a first sector of a memory and wherein the second cache memory comprises a second sector of the memory.

11. The processor of claim 10, wherein the second cache memory may be dynamically created or eliminated.

12. The processor of claim 10, wherein the size of second cache memory sector may be dynamically modified.

13. A system comprising:

a bus;

a processor coupled to the bus;

a first cache memory to support general-purpose operation for the processor; and

a second cache memory dedicated to a first program thread.

14. The system of claim 13, wherein first program thread is a multi-media process.

15. The system of claim 13, wherein the first program thread is allocated certain computing cycles of the processor.

16. The system of claim 13, wherein the first cache memory comprises a first sector of a memory unit and wherein the second cache memory comprises a second sector of the memory unit.

17. The system of claim 16, wherein the second cache memory may be dynamically created or eliminated.

18. The system of claim 16, wherein the size of second cache memory sector may be dynamically modified.

19. The system of claim 13, wherein the first cache memory and the second cache memory are included in the processor.

20. A method comprising:

storing data relating to a plurality of computer operations in a first cache memory; and

storing data regarding a first computer process in a dedicated second cache memory.

21. The method of claim 20, further comprising creating the second cache memory.

22. The method of claim 20, further comprising changing the size of the second cache memory.

23. The method of claim 20, further comprising eliminating the second cache memory.

24. The method of claim 20, further comprising flushing the first cache memory without flushing the second cache memory.

25. A machine-readable medium having stored thereon data representing sequences of instructions that, when executed by a processor, cause the processor to perform operations comprising:

storing data relating to a plurality of computer operations in a first cache memory; and

storing data regarding a first computer process in a dedicated second cache memory.

26. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising creating the second cache memory.

27. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising changing the size of the second cache memory.

28. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising eliminating the second cache memory.

29. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising flushing the first cache memory without flushing the second cache memory.